Abstract

[0054] A method and circuit for gain and/or offset correction in a CDAC circuit are provided. The gain and/or offset correction can be realized by adjusting the sampling capacitance of a capacitor array, with a positive array of the CDAC circuit being trimmed for gain correction, and a negative array of the CDAC circuit being trimmed for offset correction. Accordingly, corrections to variations in gain and/or offset caused by process variations can be suitably addressed. To facilitate gain correction, an exemplary CDAC circuit comprising an N-bit capacitor array includes on the positive side of the capacitor array an additional capacitor configured to capture the sampling voltage. .An exemplary CDAC circuit can also be configured to have one or more capacitors shifted out of the total capacitance of the capacitor array, and thus reduce the amount of charge stored during sampling. To facilitate offset correction, an exemplary CDAC circuit comprises a negative side having a capacitor array, wherein the CDAC circuit is configured to provide a desired amount of offset voltage through sampling of some of the capacitance in the negative side to a reference voltage, and sampling a remainder of the capacitance in the negative side to ground.